REMARKS

Reconsideration of this application, based on this amendment and these following remarks, is respectfully requested.

Claims 1 through 16 remain in this case. Claims 1, 4, 6, 7, 10, 15, and 16 are amended.

The specification is amended, in the first paragraph on the first page, to reflect the serial number of the related application, as requested by the Examiner. An error of a typographical nature is also corrected in this amendment to the specification. No new matter is presented.

The undersigned notes the indication that the priority document has not yet been received. On information and belief, the undersigned understands that a certified copy of the priority document is on order, and that it will be provided to the Patent and Trademark Office promptly upon its receipt.

The undersigned notes the requirement for a new executed Declaration. On information and belief, the undersigned understands that the inventors have been contacted to execute a substitute declaration, and that it will be provided to the Patent and Trademark Office promptly once the executed declaration is received.

Claims 1 through 3, 6, 8, 10, 13, and 15 were rejected under §102(b) as anticipated by the Guerra et al. reference[1]. Claims 4, 5, 7, 9, 11, 12, 14, and 16 were indicated as directed to allowable subject matter, but are objected to for depending upon rejected claims.

Claims 4 and 16 are amended to now be presented in independent form, including the elements of the claims upon which they originally depended, as suggested by the Examiner. Claim 7, dependent on claim 4, is amended for clarity. Applicants respectfully submit that amended claim 4, its dependent claims 5, 7, 9, 11, 12, and 14, and amended claim 16, are now all in condition for allowance.

Claim 1 is amended to overcome the rejection. The method of amended claim 1 now requires that the first program is executed at source hardware operating according to a first instruction set architecture, and that the second program is executed at target hardware operating according to a second instruction set architecture. Because the specification clearly supports this amendment to claim 1,[2] Applicants submit that no new matter is presented.

Claim 6 is amended for clarity.

Applicants respectfully submit that amended claim 1, and its dependent claims, are novel and patentably distinct over the Guerra et al. reference and the other prior art of record in this case. Specifically, the Guerra et al. reference fails to disclose the executing of the first program at source hardware operating according to a first instruction set architecture, and a second program at target hardware operating according to a second instruction set architecture, as required by amended claim 1.

The Guerra et al. reference is directed solely to a simulation system for modeling and verifying software for a DSP.[3] It is clear from the tenor of Section 2 of the Guerra et al. reference that its method is applied in the modeling, and system simulation, of a particular DSP.[4] It is the results of this model that are analyzed, or compared against the results of other models, in performing the verification method disclosed in the Guerra et al. reference.[5]

But nowhere does the Guerra et al. reference disclose that its method is performed by source and target hardware that execute first and second programs, respectively, according to respective first and second instruction set architectures, as required by amended claim 1, much less in a manner required by the collecting, determining, and indicating steps of the claim. Instead, the Guerra et al. reference, as mentioned above, is directed to full system simulation,

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[1] Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", *ACM* (June, 1999), pp. 964-69.
[2] Specification of S.N. 10/017,777, page 4, line 23 through page 5, line 14; Figure 1.
[3] Guerra et al., *supra,* page 964, Abstract.
[4] Guerra et al., *supra,* page 965-67, §2 (*i.e.*, §§2.1 through 2.4).
[5] *See* Guerra et al., *supra,* page 968, §4.1.

and nowhere discloses the use of source hardware and target hardware, as now required by amended claim 1 and its dependent claims.

Applicants further wish to address a factual error upon which the rejection is based. The Examiner asserts that the first and second "phases" shown in Figure 4 of the Guerra et al. reference correspond to the steps of executing first and second programs, respectively, in original claim 1.[6] Applicants respectfully traverse the rejection as based on an error in fact, to the extent it is founded on this assertion.

It is apparent from the Guerra et al. reference itself that the term "phase" refers to clock phases within an instruction or clock cycle of the simulated microprocessor. For example, the Guerra et al. reference refers to simulation traces that are "cycle/phase-accurate",[7] to the disclosed simulation solution as providing "full cycle and phase-accuracy",[8] and that to deal with instruction dependencies, the disclosed simulation method "the timing accuracy of the core model has to be increased, providing ordered cycle or even phase events".[9] This meaning of the term "phase" is consistent with its widespread use in the art.[10] Therefore, the disclosure of inputs and outputs from phases 1 and 2, as shown in Figure 4 of the Guerra et al. reference, does not correspond to the steps of executing a first program and executing a second program as recited in original claim 1, much less as recited in amended claim 1.

To the extent that the rejection of claim 1 and its dependent claims is based on this interpretation of the Guerra et al. reference, Applicants respectfully submit that the interpretation is in error and that the rejection of original claim 1 and its dependent claims is in error. Applicants further submit that this basis of the rejection remains inapplicable to claim 1, as amended.

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[6] Office Action of August 26, 2004, page 3, ¶6.
[7] Guerra et al., *supra,* page 965, right-hand column, lines 24 and 27.
[8] Guerra et al., *supra,* page 965, left-hand column, line 1.
[9] Guerra et al., *supra,* page 967, left-hand column, first full paragraph and Figure 4.
[10] *See, e.g.,* U.S. Patent No. 5,444,407, issued August 22, 1998 to Ganapathy et al., column 1, lines 22 through 49.

Applicants further respectfully submit that there is no suggestion to modify the teachings of the Guerra et al. reference in such a manner as to reach the requirements of amended claim 1 and its dependent claims. As discussed above, the Guerra et al. reference is directed solely to full system simulation of the operation of a processor in executing application program. The techniques disclosed in the Guerra et al. reference for developing its simulation model are directed purely to such simulation, and are not applicable to hardware emulation and software verification using source hardware and target hardware, operating according to first and second instruction set architectures, as required by amended claim 1. And there is no suggestion from the other prior art of record to so modify the teachings of the Guerra et al. reference.

Especially considering the important advantages of the invention of claim 1, including the automatic verification of a software application ported to another instruction set architecture by reporting discrepancies at or near the instruction at which the source and target versions vary,[11] Applicants therefore respectfully submit that amended claim 1 and its dependent claims are patentably distinct over the Guerra et al. reference and the other prior art of record in this case.

Claim 15 is amended in similar fashion as amended claim 1. Amended claim 15 is now directed to a digital system that includes a general purpose computer, first and second microprocessors, and first and second emulation hardware that control the operation of the first and second microprocessors, respectively, according to respective first and second instruction set architectures. Amended claim 15 now further requires that the general purpose program is programmed to perform the recited method steps, including causing the first emulation hardware to execute a first program at the first microprocessor, and causing the second emulation hardware to execute the second program at the second microprocessor. The specification clearly supports the amendment to claim 15,[12] and as such no new matter is presented by this amendment.

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[11] Specification, *supra,* page 4, lines 3 through 10; page 21, lines 15 through 25.
[12] Specification, *supra,* page 4, line 23 through page 5, line 14; Figure 1.

For the same reasons as discussed above relative to amended claim 1, Applicants respectfully submit that amended claim 15 is novel and patentably distinct over the Guerra et al. reference and the other prior art in this case. Nowhere does the Guerra et al. reference disclose causing first emulation hardware to execute a first program at a first microprocessor, or causing second emulation hardware to execute a second program at a second microprocessor, especially where the first and second emulation hardware control the operation of their respective microprocessors according to first and second instruction set architectures, as required by amended claim 15.

As discussed above, the Guerra et al. reference is directed solely to a simulation system for modeling and verifying software for a DSP.[13] There are no first and second microprocessors disclosed by the reference, nor are first and second emulation hardware for controlling the operation of the first and second microprocessors according to first and second instruction set architectures, respectively, disclosed by the reference, as required by amended claim 15. Failing disclosure of these hardware resources, the Guerra et al. reference necessarily fails to disclose the cooperative operation of a general purpose computer according to the other recited steps of amended claim 15. Instead, the Guerra et al. reference, as mentioned above, is directed to full system simulation.

Applicants further respectfully restate their point regarding the factual error discussed above relative to the rejection of amended claim 1, such rejection incorporated into the rejection of original claim 15.[14] As discussed above, Applicants respectfully submit that the first and second "phases" shown in Figure 4 of the Guerra et al. reference cannot correspond to the steps of executing first and second programs, respectively, in original claim 15. Instead, Applicants submit that these first and second "phases" of the reference refer to clock phases within an instruction or clock cycle of the simulated microprocessor. To the extent that the rejection of claim 15 was based on this assertion, Applicants respectfully submit that the rejection of original claim 15 was in error, and further respectfully submit that this basis of rejection is inapplicable to amended claim 15.

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[13] Guerra et al., *supra*, page 964, Abstract.

Applicants further respectfully submits that there is no suggestion to modify the teachings of the Guerra et al. reference in such a manner as to reach the requirements of amended claim 1 and its dependent claims, considering that the reference is directed solely to full system simulation of the executing of an application program. There is no suggestion from the reference, nor from the other prior art of record, to apply these disclosed techniques to a digital software verification system including first and second microprocessors and first and second emulation hardware, as required by amended claim 15. The system of amended claim 15 also provides the important advantages discussed above relative to amended claim 1, which further support the patentability of the claim.

Applicants therefore respectfully submit that amended claim 15 is patentably distinct over the Guerra et al. reference and the other prior art of record in this case.

Claim 10 is amended to be placed in independent form, incorporating thereinto the limitations of original claim 1, upon which it depended. Applicants respectfully traverse the rejection of claim 10, as made in the Office Action of August 26, 2004.

The Examiner asserted that the Guerra et al. reference discloses "the capability to determine, calculate, compute, and report as claimed".[15] Applicants first respectfully submit that disclosure of the "capability" to perform certain method steps is not disclosure of the method steps themselves. And it is the method steps that are required by claim 10, not merely the capability of performing such steps. For this reason alone, Applicants respectfully submit that the rejection of claim 10 is in error and should be withdrawn.

Further, Applicants respectfully submit that the Guerra et al. reference in fact fails to disclose or suggest the method steps required by claim 10. Specifically, among others, Applicants respectfully submit that there is no disclosure in the Guerra et al. reference of the step of finding that a valid effective address is available based on a current effective address delay, nor is there disclosure of the computing of the effective address of an instruction if a

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[14] Office Action, *supra*, page 5, ¶6.
[15] Office Action, *supra*, page 5, ¶6, *citing* Guerra et al., *supra*, page 966, section 2.3, and Figures 2 and 3.

valid effective address is not available, both steps required by claim 10. At most, the Guerra et al. reference discloses simply the delaying of interrupt handling if a conditional branch resides in the processor pipeline at the time of the interrupt.[16] There is no finding of whether a valid effective address for an instruction is available based on the current effective address delay, nor is there any computing of the effective address if a valid effective address is not available. The Guerra et al. reference therefore necessarily falls short of the requirements of claim 10, and therefore Applicants respectfully submit that claim 10 is novel over the reference.

Applicants further respectfully traverse the §102 rejection of claim 10, on the grounds that the rejection is at least partially based on a misinterpretation of the Guerra et al. reference. The Examiner carried forward, to claim 10, the bases of rejection against claim 1, including the assertion that the discussion of first and second phases in the Guerra et al. reference corresponds to the executing of first and second programs, as required by claim 10. As discussed above, Applicants submit that the first and second phases disclosed by the reference refer to first and second phases within an instruction cycle, and cannot correspond to first and second programs being executed. Accordingly, to the extent that the rejection of claim 10 is based on this error in fact, Applicants respectfully traverse the rejection.

Applicants further respectfully submit that there is no suggestion from the Guerra et al. reference nor from the other prior art of record of the method of amended claim 10. There is simply no suggestion of the particular steps used to collect the first and second sets of events, as recited by amended claim 10. The greatly improved visibility into the operation of the application program being verified, as provided by the inventive method of claim 10, further supports the patentability of this claim.

For these reasons, Applicants respectfully submit that amended claim 10 is novel and patentably distinct over the prior art of record in this case.

Applicants also wish to bring the information listed on the enclosed PTO/SB/08B to the attention of the Patent and Trademark Office in connection with this application.

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[16] Guerra et al., *supra*, page 966, right-hand column, lines 40 through 49.

A copy of each reference is enclosed. The references are all in the English language. As such, no additional statement of relevance is provided in this paper.[17] Some of these references were cited in an Office Action in copending application S.N. 10/011,777, to which reference is made on page 1 of the specification of this application (as amended).

While this information is being cited after a first Office Action on the merits in this application, this information is cited prior to a final action, allowance, or other close of prosecution of this application. The fee set under 37 C.F.R. §1.17(p) is paid by way of the enclosed Fee Transmittal. Applicants therefore submit that this information is timely cited.[18]

By citing these references, Applicants do not admit that any of these references is, or is considered to be, material to the patentability of any of the claims of this application.[19]

The prior art cited as pertinent by the Examiner, but not applied against the claims, has been considered but is not felt to come within the scope of the claims in this case.

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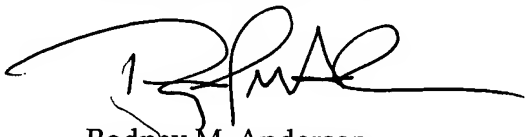
[17] 37 C.F.R. §1.97(3)(i).
[18] 37 C.F.R. §1.97(c).
[19] 37 C.F.R. §1.97(h).

For these reasons, Applicants respectfully submit that all claims now in this case are in condition for allowance. Reconsideration of this application is therefore respectfully requested.

Respectfully submitted,



Rodney M. Anderson

Registry No. 31,939

Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.

14785 Preston Road, Suite 650

Dallas, Texas 75254

(972) 664-9554

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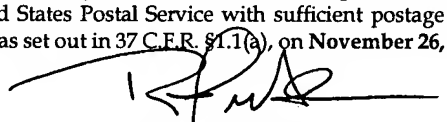

Rodney M. Anderson
Registry No. 31,939